REMARKS

Reconsideration of the application is respectfully requested.

Claims 1-16 are pending and remain in this application. No claims have been added, amended or cancelled. Claims 1-14 were filed with the application and were reconsidered in the Office Action while claims 15 and 16 were presented in Applicant's Response to Office Action dated October 24, 2003.[1]

Rejections Under 35 U.S.C. § 103

The Office Action has rejected claims 1, 2, 5-10, 13 and 14 under 35 U.S.C. § 103(a) as being unpatentable over Beausoleil et al. U.S. Patent 5,551,013 (hereinafter "Beausoleil") in view of Sarno et al. U.S. Patent 6,141,636 (hereinafter "Sarno"). Applicant respectfully traverses this rejection.

Applicant initially notes that the Office Action's definition of "wave logic" is not correct. Specifically, the Office Action defines "wave logic" to be logic that generates "a collection of control signals sent to cells in a FPGA that are being used in a processor emulation to enable emulation functionality from the combination of compiled test bench data with actual logic functionality for the purpose of improving the speed of the emulation/simulation." This cannot be the case since processor emulation systems use processors, not FPGAs. Moreover, test bench signals and actual logic functionality would not be combined to increase emulation speed. Test bench signals are run in an emulator that is emulating a logic design.

[1] The "Office Action Summary" states that only claims 1-14 are currently pending, which is not correct. Page 2 of the Detailed Action accurately summarizes which claims are pending.

Applicant also notes the following, which demonstrates that the rejection should be withdrawn. The Office Action states at page 4, lines 8-12 as follows:

> ... the *Sarno et al.* reference teaches ... the plurality of cells arraigned in rows and columns ... (Figure 1, 2, 14, and 15) ...

Applicant surmises that the Office Action is arguing that 48:1 selectors at 152, shift registers at 152, 1K:1 selectors at 158, and HLUs at 162 in figure 14[2] correspond to "the plurality of cells arraigned in rows and columns", because Applicant cannot find anything like cells in figures 1, 2, and 15. However, these components in figure 14 also do not correspond to the cells defined by the claims of the present application. This is due to the fact that in Sarno, the number of 48:1 selectors and shift registers at reference numeral 152, 1K:1 selectors at reference numeral 158 and HLUs at reference numerals 162 are respectively 255, 255, 127 and 7 (see figure 14), which means that these components are not arranged in S rows and P columns as required by claims 1 and 9.

In addition, Sarno does not disclose that the components shown in figure 14 comprise a configurable logic function memory specifying a logic function of a plurality of input lines, which is required by claims 1 and 9. Though figure 2 shows that "state storage" is part of processor chip 208, there is no description anywhere in Sarno about what this "state storage" does. Therefore, the meaning of the storage referred to in Sarno is unclear and certainly does not teach that the storage is used to specify logic functions. Meanwhile, the Office Action states that Beausoleil discloses such a configurable logic function memory. However, even if the memory

[2] 48:1 selectors at 152 correspond to selectors 110 in figure 13. Shift registers at 152 correspond to registers 108 in figure 13. 1K:1 selectors at 158 correspond to selectors 106 in figure 13. HLUs at 162 correspond to HLUs 112 in figure 13.

is disclosed in Beausoleil, both Beausoleil and Sarno state no motivation to combine each of these components of figure 14 in Sarno with the memory in Beausoleil.

Next, the Office Action states at page 4, lines 8-14 as follows:

> ... the *Sarno et al.* reference teaches ...
> sequential signals corresponding to a row of cells and controlling propagation of logic signals through the cells of that row (Figure 1, 2, 14, and 15), as well as "*wave logic*" signals used to control and reconfigure the emulation resources on an *as needed* basis (Figure 13, item 102, Figure 16 Items 222 & 220, Figure 18 "EMULATION MEMORY").

Here, Applicant respectfully notes that claims 1 and 9 require:

> (1) wave logic for producing a plurality of sequential wave signals,
> (2) each wave signal corresponding to a row of cells,
> (3) each wave signal controlling the propagation of logic signals through the cells of the row.

In other words, claims 1 and 9 require that each wave signal "produced by wave logic" corresponds to a row of cells and that these wave signals control the propagation of logic signals through the cells of the row. Here, Applicant surmises that the Office Action means that signals passing at 150 in figure 14 (i.e., signals input to 48:1 selectors 110 in figure 13) correspond to the "sequential signals" required by the claims, and the "wave logic" also required by the claims is located on HLU 112 in figure 13. In order for these teachings to supply the limitations required by claims 1 or 9, it is necessary for inputs of 48:1 selectors 110 to be related to the outputs of HLUs 112. However, some of the signals 150 are input from outside of chip 100, which means outside of HLUs 112 (see figure 13). In other words, at least some inputs of 48:1 selectors are not related to outputs of HLUs 112. Thus, Sarno does not teach "wave logic" as required by claims 1 and 9.

In addition, the Office Action states that "control data" block 102 of Sarno discloses the "wave logic" required by claims 1 and 9. Applicant respectfully disagrees. The claims require

that the wave logic produce "wave signals" that control the *propagation* of logic signals through the cells of each row. In contrast, Sarno teaches that the control data block 102 provides "control words" to the functional blocks on the chip. According to Sarno, "control words" "are routed, by means of control lines, to other functional blocks on the chip to control, e.g., n:1 selectors, shift registers, pass gates, signal inversion..." (col. 9, lines 27-29). As seen in Fig. 13 of Sarno, these selectors, shift registers, etc., are not even located in the HLU array 114 (The HLUs are shown in greater detail in Fig. 14). Thus, the control data block 102 of Sarno cannot control the *propagation* of logic signals through rows as required by the claims since it is not even located in a position where the control could be affectuated.

Thus, Sarno does not teach "wave logic" as required by claims 1 and 9. As demonstrated, the teachings found in Sarno referred to in the Office Action states are quite different from the subject matter of claims 1 and 9. Thus, even if Beausoleil and Sarno are properly combinable, the combination does not teach all elements of claims 1 and 9. Consequently, Applicant respectfully submits the subject matter of claims 1 and 9 would not have been obvious at the time the invention was made to a person having ordinary skill in the art regardless of whether or not there is motivation to combine them.

Claims 2, 5-8, 10, 13 and 14 are allowable because they depend either directly or indirectly from claim 1 (claims 2 and 5-8) or claim 9 (claims 10, 13 and 14), which are allowable.

Applicant acknowledges that the Office Action has objected to claims 3, 4, 11, 12, 15 and 16 as being dependent upon rejected base claims 1, 9. However, because claims 1 and 9 are allowable for the reasons discussed above, Applicant respectfully submits that this objection has been overcome and that claims 3, 4, 11, 12, 15 and 16 need not be rewritten in order to obtain allowance.

Based on the foregoing, Applicant respectfully submits that the subject application is in condition for allowance. The Applicant therefore respectfully requests that the subject application be allowed.

Should the Examiner have any questions or comments on the application, the undersigned can be reached at (650) 614-7660.

Respectfully submitted,
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Dated: April 29, 2004 By: _____

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